WHAT IS CLAIMED IS:

1. A circuit comprising:

a phase detector circuit receiving a reference clock signal and a feedback clock signal;

a charge pump circuit coupled to the phase detector circuit; and

a voltage controlled oscillator coupled to the charge pump, wherein the voltage controlled oscillator comprises,

a first multiplexer having inputs coupled to first and second outputs of the voltage controlled oscillator,

a first variable impedance circuit coupled to a third output of the voltage controlled oscillator and the charge pump circuit, and

a first capacitance coupled to the first variable impedance circuit.

2. The circuit of claim 1 wherein the voltage controlled oscillator further comprises:

a second multiplexer having inputs coupled to the third output and a fourth output of the voltage controlled oscillator;

a second variable impedance circuit coupled to the second output of the voltage controlled oscillator and the charge pump circuit; and

a second capacitance coupled to the second variable impedance circuit.

3. The circuit of claim 2 wherein the first and the second variable impedance circuits each comprise a transistor that has a gate coupled to the charge pump circuit.

4. The circuit of claim 2 wherein the voltage controlled oscillator further comprises:

a third multiplexer having inputs coupled to the third output and the fourth output of the voltage controlled oscillator;

a third variable impedance circuit coupled to the fifth output of the voltage controlled oscillator and to the charge pump; and

a third capacitance coupled to the third variable impedance circuit.

5. The circuit of claim 1 further comprising a level shift circuit coupled between the voltage controlled oscillator and the charge pump circuit.

6. A method for generating an output clock signal, the method comprising:

generating a signal indicative of a phase difference between a reference clock signal and a feedback clock signal;

adjusting an output signal of a charge pump in response to the phase difference signal;

selecting a first signal or a second signal to provide a third signal using a first multiplexer, wherein the first, the second, and the third signals are output signals of a voltage controlled oscillator;

providing a delay to the third signal that is based on a first capacitance; and

varying an impedance of a first variable impedance circuit in response to the output signal of the charge pump to vary the first capacitance.

7. The method of claim 6 further comprising:

selecting the third signal or a fourth signal to provide the second signal using a second multiplexer;

providing a delay to the second signal based on a second capacitance; and

varying an impedance of a second variable impedance circuit in response to the output signal of the charge pump to vary the second capacitance.

8. The method of claim 7 further comprising:

selecting the third signal or the fourth signal to provide a fifth signal using a third multiplexer;

providing a delay to the fifth signal that is based on a third capacitance; and

varying an impedance of a third variable impedance circuit in response to the output signal of the charge pump to vary the third capacitance.

9. The method of claim 8 further comprising:

selecting the fifth signal or a sixth signal to provide the fourth signal using a fourth multiplexer;

providing a delay to the fourth signal that is based on a fourth capacitance; and

varying an impedance of a fourth variable impedance circuit in response to the output signal of the charge pump to vary the fourth capacitance.

10. A method for generating an output clock signal, the method comprising:

generating a signal indicative of a phase difference between a reference clock signal and a feedback clock signal using a phase detector;

generating a signal from a charge pump in response to the signal from the phase detector;

providing a delay to a first output signal of a voltage controlled oscillator that is based on a first capacitance;

adjusting the frequency of the first output signal by varying an impedance of a first variable impedance circuit in response to the charge pump signal; and

providing the first output signal of the voltage controlled oscillator as the output clock signal.

11. The method of claim 10 further comprising:

providing a delay to a second output signal of the voltage controlled oscillator that is based on a second capacitance, wherein the second capacitance is coupled to a second variable impedance circuit that is responsive to the charge pump signal.

12. The method of claim 11 wherein the voltage controlled oscillator includes:

a first multiplexer coupled to the first variable impedance circuit; and

a second multiplexer coupled to the second variable impedance circuit.

13. The method of claim 11 further comprising:

providing a delay to a third output signal of the voltage controlled oscillator that is based on a third capacitance, wherein the third capacitance is coupled to a third variable impedance circuit that is responsive to the charge pump signal.

14. The method of claim 13 further comprising:

selecting from among the first, the second, and the third output signals of the voltage controlled oscillator to provide the feedback clock signal.